`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 23.01.2020 09:50:08

// Design Name:

// Module Name: max\_pool\_b

// Project Name:

// Target Devices:

// Tool Versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module max\_pool\_b #(parameter m=32,parameter n=4)(

input [m-1:0] a,

input clk,

input en,

input [n-1:0] addr,

output [m-1:0] out

//output reg[m-1:0] max\_m

);

reg[m-1:0]a1[m:0];

reg[m-1:0] max\_m;

integer i;

always@(posedge clk)begin

// if(en)

// a1[addr]<=8'b0;

//else

a1[addr]<=a;

end

always@(posedge clk)begin

if(en)

max\_m<=32'b0;

else begin

for(i=0;i<9;i=i+1)begin

// if(a1[i]>a1[i+1])

//a1[i+1]<=a1[i];

if(a1[i]>=max\_m)

max\_m<=a1[i];

else

max\_m<=max\_m;

//a1[i+1]<=a1[i+1];

end

end

end

//assign out=en ? 8'b0:a1[8];

assign out=en ? 32'b0:max\_m;

endmodule